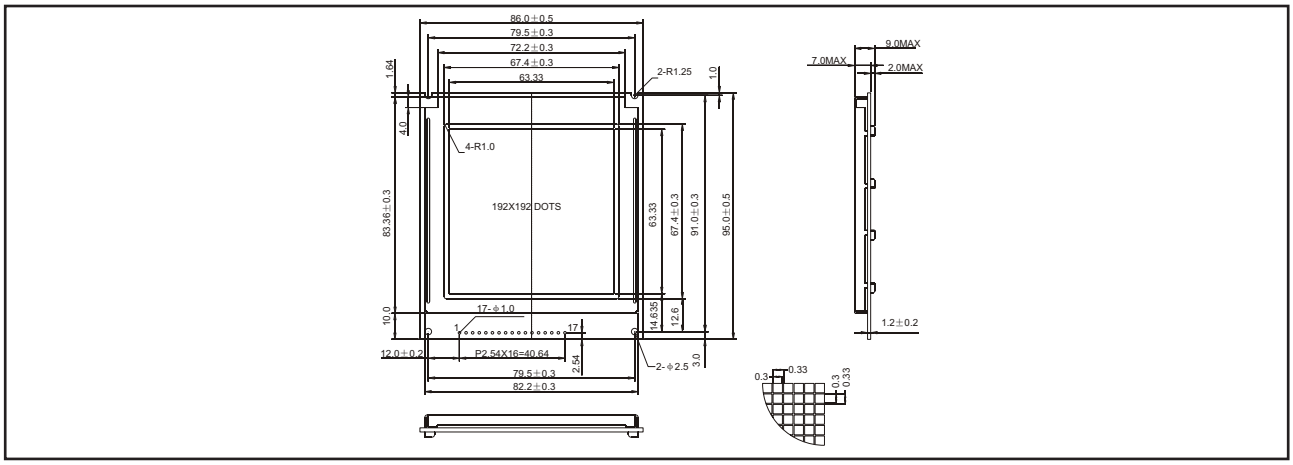
STANDARD GRAPHIC MODULES

YMC 192192-01

192 X 192 DOTS, 1/192 DUTY, 1/12 BIAS

EXTERNAL DIMENSION AND DISPLAY PATTERN



MECHANICAL DATA

ITEM	SPECIFICATION	UNIT
Module Size (W x H x T)	86.0 x 95.0 x 9.0	mm
Viewing Area (W x H)	67.4 x 67.4	mm
Number of Dots	192 x 192	dots
Dot Pitch (W x H)	0.33 x 0.33	mm
Dot Size (W x H)	0.3 x 0.3	mm

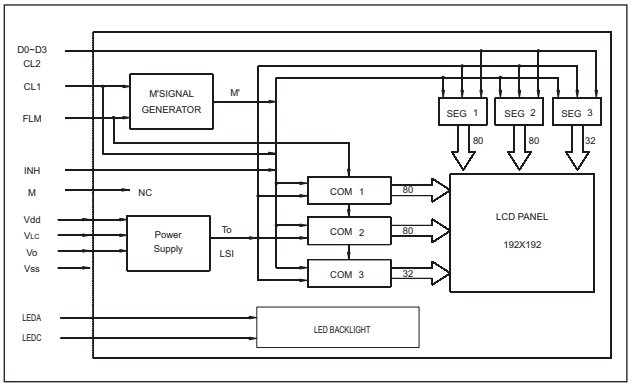
ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage Logic	V_{DD} - V_{SS}	-0.3	7.0	V
Supply Voltage Drive	V_{DD} - V_{EE}	-0.3	30.0	V
Input Voltage	V_{IN}	-0.3	V_{DD} +0.3	V
Operating Temperature	See page 8			
Storage Temperature				

PIN CONFIGURATION

PIN	SYMBOL	SIGNAL DESCRIPTION
1	V_{DD}	Logic Supply Voltage (+5.0V)
2	FG	Frame Ground
3	CL2	Data Shift Clock
4	INH	Display ON/OFF Control Terminal
5	FLM	Frame Signal
6	CL1	Data Latch Signal
7	V_{SS}	GND
8	M	LCD Drive Signal (AC Signal)
9-12	DB_0-DB_3	Data Bus Line
13	V_{LC}	Operating Voltage for LCD
14	V_0	LCD Drive Output Voltage Level
15	V_{SS}	GND
16	LEDA	Power Supply Terminal for Driving LED Backlight
17	LEDC	GND Terminal for Driving LED Backlight

BLOCK DIAGRAM



BACKLIGHTING CHARACTERISTICS, Ta = 25°C, LED

ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
Supply Voltage	V_F	I_F=150mA	3.9	4.1	4.3	V
Power Consumption	P_{LED}			615		mW

ELECTRICAL CHARACTERISTICS, Ta = 25°C

ITEM		SYMBOL	CONDITION	SPEC. VALUE			UNIT
				MIN.	TYP.	MAX.	
Supply Voltage (Logic)		V_{DD} - V_{SS}		2.7	5.0	5.5	V
Supply Current (Logic)		I_{DD}	V_{DD} =5V		0.8		mA
Input Voltage	HIGH	V_{IH}		0.8 V_{DD}		V_{DD}	V
	LOW	V_{IL}				0.2 V_{DD}	V
Output Voltage	HIGH	V_{OH}		V_{DD} -0.4			V
	LOW	V_{OL}				0.4	V
LCD Operating Voltage		V_{DD} - V_{EE}	V_{DD} =5V Ta=+25°C	6.0	24.0	28.0	V
Supply Current LCD Drive		I_{EE}			0.5		mA

Note (1): Value is high reliability type. Note (2): Electro-Optical Characteristics: See page 5.

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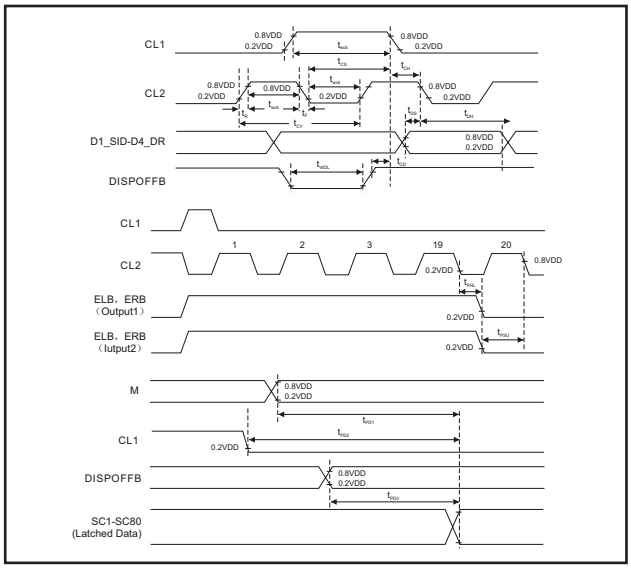
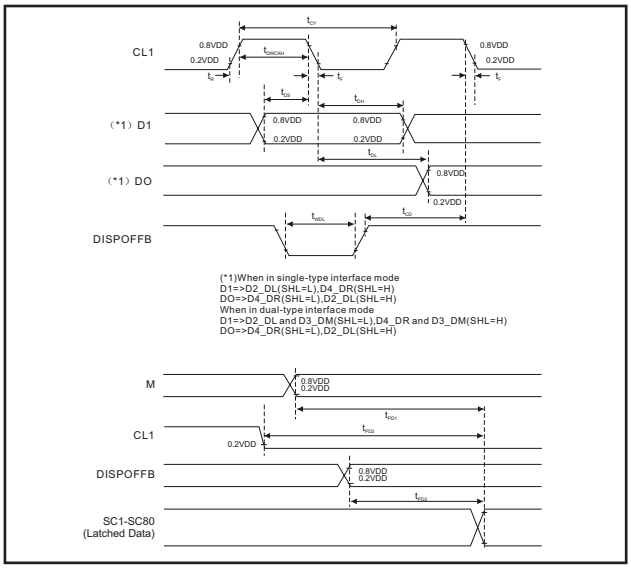
SEGMENT DRIVER APPLICATION TIMING



COMMON DRIVER APPLICATION TIMING



(*1)When in single-type interface mode
D1=>D2_DL(SHL=L),D4_DR(SHL=H)
DO=>D4_DR(SHL=L),D2_DL(SHL=H)
When in dual-type interface mode
D1=>D2_DL and D3_DM(SHL=L),D4_DR and D3_DM(SHL=H)
DO=>D4_DR(SHL=L),D2_DL(SHL=H)

AC CHARACTERISTICS: SEGMENT DRIVER APPLICATION, V_{SS}= 0V , Ta=-30°C to +85°C

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}= 5V ±10% (1)			V_{DD}= 3V ±10% (2)			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Clock Cycle Time	t_{CY}	Duty=50%	125			250			ns
Clock Pulse Width	t_{WCK}		45			95			ns
Clock Rise / Fall Time	t_R/t_F							30	ns
Data Setup Time	t_{DS}		30			65			ns
Data Hold Time	t_{DH}		30			65			ns
Clock Setup Time	t_{CS}		80			120			ns
Clock Hold Time	t_{CH}		80			120			ns
Propagation Delay Time	t_{PHL}	ELB Output			60			125	ns
		ERB Output			60			125	ns
ELB ERB Setup Time	t_{PSU}	ELB Input	30			65			ns
		ERB Input	30			65			ns
DISPOFFB Low Pulse Width	t_{WDL}		1.2			1.2			µs
DISPOFFB Clear Time	t_{CD}		100			100			ns
M-OUT Propagation Delay Time	t_{PD1}	C_L=15pF			1.0			1.2	µs
CLI-OUT Propagation Delay Time	t_{PD2}				1.0			1.2	µs
DISPOFFB-OUT Propagation Delay Time	t_{PD3}				1.0				µs

AC CHARACTERISTICS: COMMON DRIVER APPLICATION, V_{SS}= 0V , Ta=-30°C to +85°C

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}= 5V ±10% (1)			V_{DD}= 3V ±10% (2)			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Clock Cycle Time	t_{CY}	Duty=50%	250			500			ns
Clock Pulse Width	t_{WCK}		45			95			ns
Clock Rise / Fall Time	t_R/t_F				50			50	ns
Data Setup Time	t_{DS}		30			65			ns
Data Hold Time	t_{DH}		30			65			ns
DISPOFFB Low Pulse Width	t_{WDL}		1.2			1.2			µs
DISPOFFB Clear Time	t_{CD}		100			100			ns
Output Delay Time	t_{DL}	C_L=15pF			200			250	ns
M-OUT Propagation Delay Time	t_{PD1}				1.0			1.2	µs
CLI-OUT Propagation Delay Time	t_{PD2}				1.0			1.2	µs
DISPOFFB-OUT Propagation Delay Time	t_{PD3}				1.0			1.2	µs