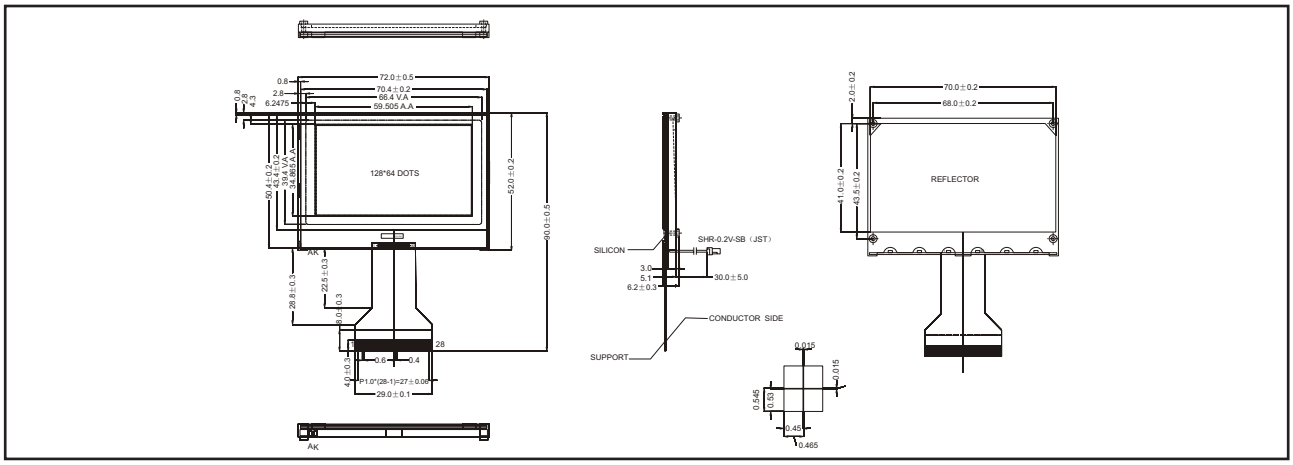
STANDARD COG MODULES

YMS 12864-18

128 X 64 DOTS, 1/64 DUTY, 1/9 BIAS

EXTERNAL DIMENSION AND DISPLAY PATTERN



MECHANICAL DATA

ITEM	SPECIFICATION	UNIT
Module Size (W x H x T)	72.0 x 90.0 x 7.0	mm
Viewing Area (W x H)	66.4 x 39.4	mm
Number of Dots	128 x 64	dots
Dot Pitch (W x H)	0.465 x 0.545	mm
Dot Size (W x H)	0.45 x 0.53	mm

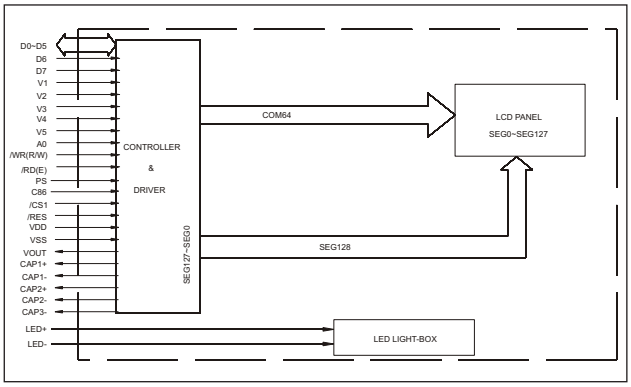
ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage Logic	V_{DD} - V_{SS}	-0.3	7.0	V
Supply Voltage Drive	V_{DD} - V_{EE}	-0.3	30.0	V
Input Voltage	V_{IN}	-0.3	V_{DD} +0.3	V
Operating Temperature	See page 8			
Storage Temperature				

PIN CONFIGURATION

PIN	SYMBOL	SIGNAL DESCRIPTION
1	P/S	Parallel / Serial Data Input Select Input
2	C_{86}	Microprocessor Interface Select Input Signal in Parallel Mode
3-7	V_5-V_1	LCD Driver Supply oltges
8-9	CAP_{2+}, CAP_{2-}	Capacitor 2 Positive/Negative Connection Pin for Voltage Converter
10-11	CAP_{1+}, CAP_{1-}	Capacitor 1 Positive/Negative Connection Pin for Voltage Converter
12	CAP_{3-}	Capacitor 3 Negative Connection Pin for Voltage Converter
13	V_{OUT}	Voltage Converter Input / Output Pin
14	V_{SS}	Ground
15	V_{DD}	Power Supply
16	D_7 (SI)	Data Bit 7 (Serial Input Data)
17	D_6 (SCL)	Data Bit 6 (Serial Input Clock)
18-23	D_5-D_0	Data Bit 5 - Data Bit 0
24	/RD (E)	Read Execution Control (Enable)
25	/WR (R/W)	Write Execution Control (Read / Write)
26	A_0	H: Data, L: Instruction Code
27	/RES	Reset Signal
28	$/CS_1$	Chip Select Signal

BLOCK DIAGRAM



BACKLIGHTING CHARACTERISTICS, Ta = 25°C, LED

ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
Supply Voltage	V_{LED}	I_F=90mA	2.85	3.2	3.4	V
Power Consumption	P_{LED}	I_F=90mA		288	306	mW
Luminous				60		cd/m^2

ELECTRICAL CHARACTERISTICS, Ta = 25°C

ITEM		SYMBOL	CONDITION	SPEC. VALUE			UNIT
				MIN.	TYP.	MAX.	
Supply Voltage (Logic)		V_{DD} - V_{SS}		2.7		3.3	V
Supply Current (Logic)		I_{DD}	V_{DD} =3.3V	0.8		1.2	mA
Input Voltage	HIGH	V_{IH}		V_{DD} -2.2		V_{DD}	V
	LOW	V_{IL}		0		0.8	V
Output Voltage	HIGH	V_{OH}		V_{DD} -0.3		V_{DD}	V
	LOW	V_{OL}		0		0.3	V
LCD Operating Voltage		V_{DD} - V_{EE}	V_{DD} =3.3V Ta=+25°C		9.7		V
Supply Current LCD Drive		I_{EE}		0.7		1.0	mA

Note (1): Value is high reliability type.

Note (2): Electro-Optical Characteristics: See page 5.

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All specifications subject to change without notice.

STANDARD COG MODULES

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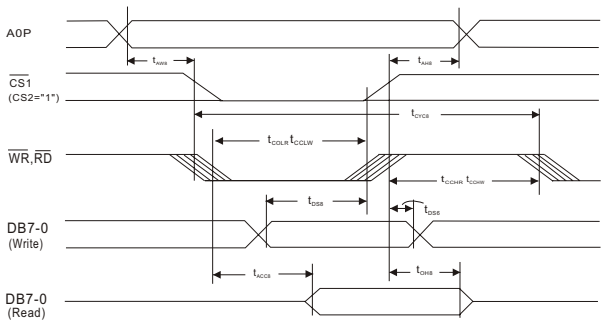
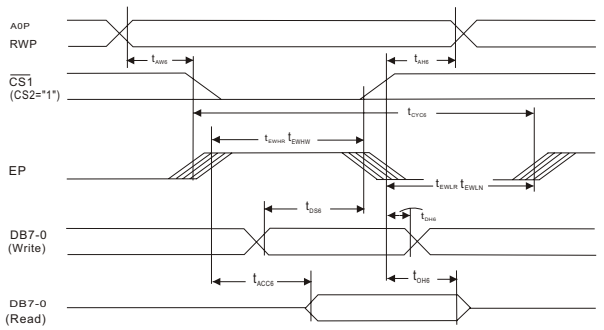
INTERFACE TIMING CHARACTERISTICS

System Bus Read / Write Characteristics 1 (8080 Series MPU)



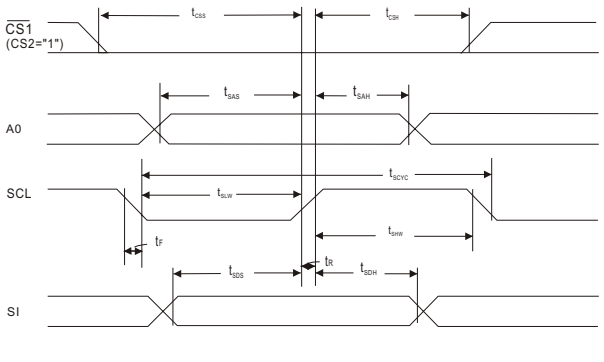
Test Conditions: V_{DD}= 2.7V to 4.5V, Ta=-25°C						
PARAMETER	SIGNAL	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Address Hold Time	AOP	t_{AH8}		0		ns
Address Setup Time		t_{AW8}		0		ns
System Cycle Time	AOP	t_{CYC8}		300		ns
Control L Pulse Width	/WR	t_{CCLW}		60		ns
Control L Pulse Width	/RD	t_{CCLR}		120		ns
Control H Pulse Width	/WR	t_{CCHW}		60		ns
Control H Pulse Width	/RD	t_{CCHR}		60		ns
Data Setup Time	$DB_{7\ to}\ DB_0$	t_{DS8}		40		ns
Address Hold Time		t_{DH8}		15		ns
RD Access Time		t_{ACC8}	C_L=100pF		140	ns
Output Disable Time		t_{CH8}		10	100	ns

System Bus Read / Write Characteristics 2 (6800 Series MPU)



Test Conditions: V_{DD}= 2.7V to 4.5V, Ta=-25°C							
PARAMETER		SIGNAL	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Address Hold Time		AOP	t_{AH6}		0		ns
Address Setup Time			t_{AW6}		0		ns
System Cycle Time		AOP	t_{CYC6}		300		ns
Data Setup Time		$DB_{7\ to}\ DB_0$	t_{DS6}	C_L=100pF	40		ns
Address Hold Time			t_{DH6}		15		ns
RD Access Time			t_{ACC6}			140	ns
Output Disable Time			t_{CH6}		10	100	ns
Enable H Pulse Time	Read	EP	t_{EWHR}		120		ns
	Write		t_{EWHW}		60		ns
Enable L Pulse Time	Read	EP	t_{EWLR}		60		ns
	Write		t_{EWLW}		60		ns

The Serial Interface



Test Conditions: V_{DD}= 2.7V to 4.5V, Ta=-25°C						
PARAMETER	SIGNAL	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Senal Clock Period	SCL	t_{SCYC}		250		ns
SCL „H“ Pulse Width		t_{SHW}		100		ns
SCL „L“ Pulse Width		t_{SLW}		100		ns
Address Setup Time	AOP	t_{SAS}		150		ns
Address Hold Time		t_{SAH}		150		ns
Data Setup Time	SI	t_{SDS}		100		ns
Data Hold Time		t_{SOH}		100		ns
CS-SCL Time	CS	t_{CSS}		150		ns
		t_{CSH}		150		ns