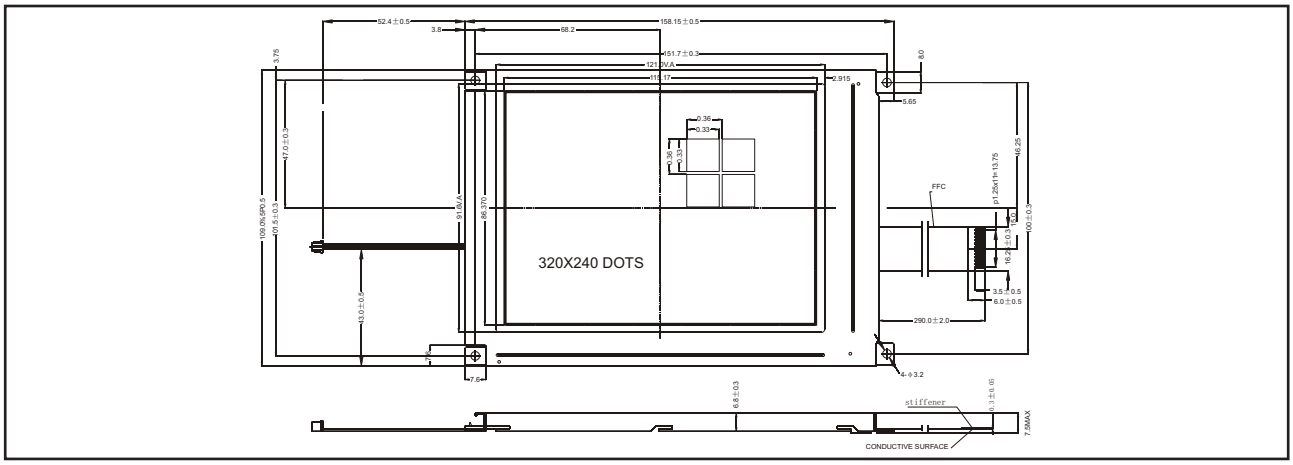
STANDARD TAB MODULES

YMS 320240-12

320 X 240 DOTS, 1/240 DUTY, 1/12 BIAS

EXTERNAL DIMENSION AND DISPLAY PATTERN



MECHANICAL DATA

ITEM	SPECIFICATION	UNIT
Module Size (W x H x T)	158.15 x 109.0 x 7.5	mm
Viewing Area (W x H)	121.0 x 91.6	mm
Number of Dots	320 x 240	dots
Dot Pitch (W x H)	0.33 x 0.36	mm
Dot Size (W x H)	0.33 x 0.33	mm

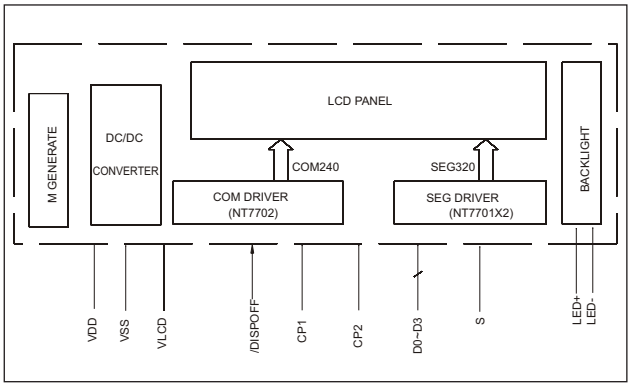
ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage Logic	V_{DD} - V_{SS}	-0.3	7.0	V
Supply Voltage Drive	V_{DD} - V_{EE}	-0.3	30.0	V
Input Voltage	V_{IN}	-0.3	V_{DD} +0.3	V
Operating Temperature	See page 8			
Storage Temperature				

PIN CONFIGURATION

PIN	SYMBOL	SIGNAL DESCRIPTION
1	S	Frame Signal
2	CP_1	Latch Pulse Input Pin for Display Data
3	CP_2	Clock Input Pin for Tking Display Data
4	NC	No Connection
5	DISP.OFF	Control Input Pin for Output Deselect Level
6-9	DB_0-DB_3	Data Bit 0 - Data Bit 3
10	V_{DD}	Power Supply for Logic
11	GND	Ground
12	V_{LCD}	Power Supply Pin for LCD Driver Voltage

BLOCK DIAGRAM



BACKLIGHTING CHARACTERISTICS, Ta = 25°C, LED

ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
Forward Current	IF	VF=3.2V		120		mA
Power Consumption	P_{LED}			384		mW
Luminous				TBD		cd/m^2

ELECTRICAL CHARACTERISTICS, Ta = 25°C

ITEM		SYMBOL	CONDITION	SPEC. VALUE			UNIT
				MIN.	TYP.	MAX.	
Supply Voltage (Logic)		V_{DD} - V_{SS}		2.5	5.0	5.5	V
Supply Current (Logic)		I_{DD}	V_{DD} =5.0V			2.0	mA
Input Voltage	HIGH	V_{IH}		0.8 V_{DD}			V
	LOW	V_{IL}				0.2 V_{DD}	V
Output Voltage	HIGH	V_{OH}		V_{DD} -0.4			V
	LOW	V_{OL}				0.4	V
LCD Operating Voltage		V_{DD} - V_{EE}	V_{DD} =5.0V Ta=+25°C		21.9		V
Supply Current LCD Drive		I_{EE}				1.4	mA

Note (1): Value is high reliability type.

Note (2): Electro-Optical Characteristics: See page 5.

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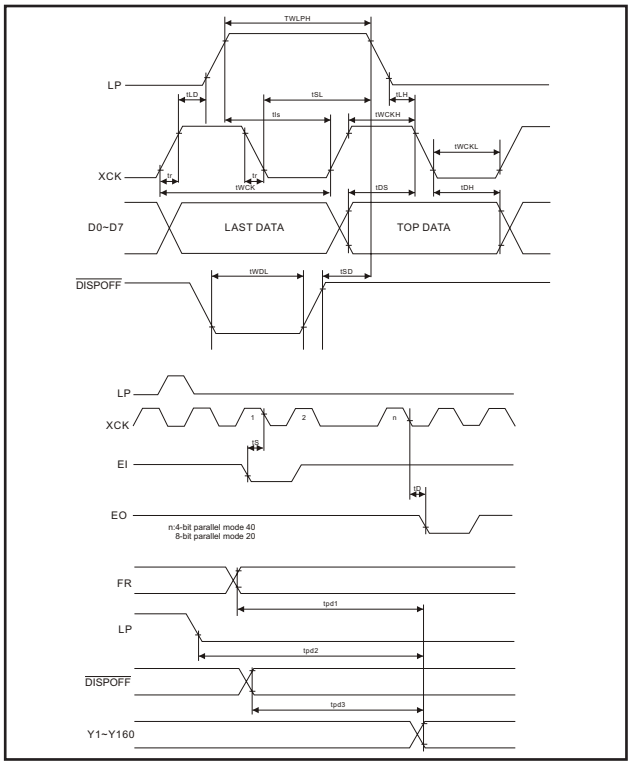
TIMING WAVEFORM OF SEGMENT MODE

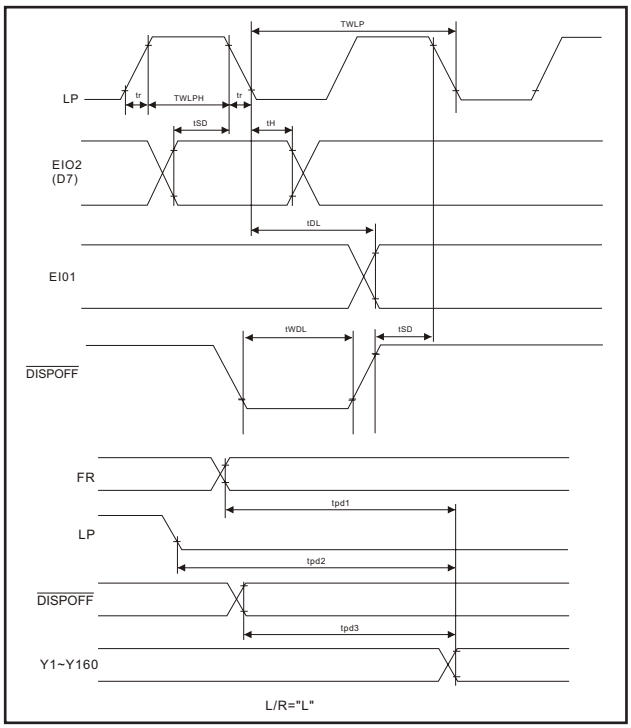


SEGMENT MODE

V_{SS}=0V, V_{DD}=2.5~4.5V, V_0=15 to 30V, Ta=-20°C to +85°C, unless othewise noted.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Shift Clock Period	t_{WCK}	71			ns	tr, tr≤11ns Note 1
Shift Clock „H" Pulse Width	t_{WCKH}	23			ns	
Shift Clock „L" Pulse Width	t_{WCKL}	23			ns	
Data Setup Time	t_{DS}	10			ns	
Data Hole Time	t_{DH}	20			ns	
Latch Pulse „H" Pulse Width	t_{WLPH}	23			ns	
Shift Clock Rise to Latch Pulse Rise Time	t_{LD}	0			ns	
Shift Clock Fall to Latch Pulse Fall Time	t_{SL}	25			ns	
Latch Pulse Rise to Shift Clock Rise Time	t_{LS}	25			ns	
Latch Pulse Fall to Shift Clock Fall Time	t_{LH}	25			ns	
Input Signal Rise Time	t_r			50	ns	Note 2
Input Signal Fall Time	t_f			50	ns	Note 2
Enable Setup Time	t_S	21			ns	
/DISPOFF Remoal Time	t_{SD}	100			ns	
/DISPOFF Enable Pulse Width	t_{WDL}	1.2			ns	
Output Delay Time (1)	t_D			40	ns	C_L=15pF
Output Delay Time (2)	t_{pd1}, t_{pd2}			1.2	µs	C_L=15pF
Output Delay Time (3)	t_{pd3}			1.2	µs	C_L=15pF

TIMING CHARACTERISTICS OF COMMON MODE



COMMON MODE

V_{SS}=0V, V_{DD}=2.5~5.5V, V_0=15 to 30V, Ta=-20°C to +85°C, unless othewise noted.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Shift Clock Period	t_{WLP}	250			ns	tr, tr≤20ns Note 1
Shift Clock „H" Pulse Width	t_{WLPH}	15			ns	V_{DD}=+5.0V +/-10%
		30			ns	V_{DD}=+2.5 ~+4.5V
Data Setup Time	t_{SU}	30			ns	
Data Hole Time	t_H	50			ns	
Input Signal Rise Time	t_r			50	ns	
Input Signal Fall Time	t_f			50	ns	
/DISPOFF Remoal Time	t_{SD}	100			ns	
/DISPOFF Enable Pulse Width	t_{WDL}	1.2			ns	
Output Delay Time (1)	t_D			200	ns	C_L=15pF
Output Delay Time (2)	t_{pd1}, t_{pd2}			1.2	µs	C_L=15pF
Output Delay Time (3)	t_{pd3}			1.2	µs	C_L=15pF