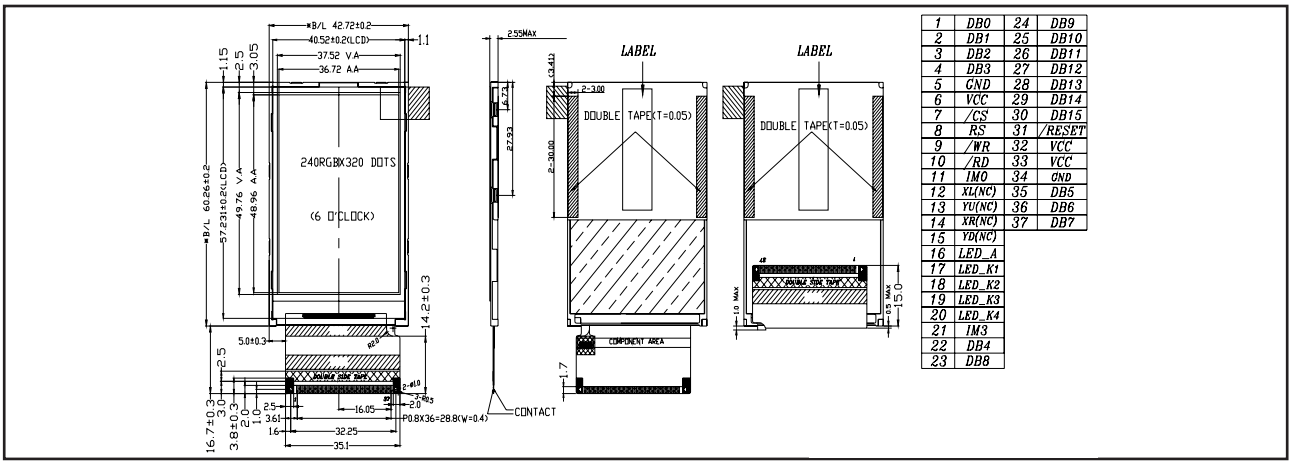
TFT TRANSMISSIVE LCD MODULES

YTS 240DLAG-01-102N

2.4'', 240 X 320 DOTS, 1/320 DUTY

EXTERNAL DIMENSION AND DISPLAY PATTERN



1	DB0	24	DB9
2	DB1	25	DB10
3	DB2	26	DB11
4	DB3	27	DB12
5	GND	28	DB13
6	VCC	29	DB14
7	/CS	30	DB15
8	RS	31	/RESET
9	/WR	32	VCC
10	/RD	33	VCC
11	IM0	34	GND
12	XL(NC)	35	DB5
13	YU(NC)	36	DB6
14	XR(NC)	37	DB7
15	YD(NC)		
16	LED_A		
17	LED_K1		
18	LED_K2		
19	LED_K3		
20	LED_K4		
21	IM3		
22	DB4		
23	DB8		

MECHANICAL DATA

ITEM	SPECIFICATION	UNIT
Module Size (W x H)	42.72 x 60.26 x 2.55	mm
Active Area (W x H)	36.72 x 48.96	mm
Viewing Direction	6:00	o´clock
Number of Dots	240 (RGB) x 320	dots
Colors	262K	

Note (1): GND must be maintained. High $V_{CI} \geq$ GND (Low), (High) $IOV_{CC} \geq$ GND (Low). Mke sure (High): $V_{CI} \geq$ GND (Low); $DDV_{DH} \geq$ GND (Low); $DDV_{DH} \geq V_{CL}$ (Low); $V_{GH} \geq$ GND (Low); GND $\geq V_{GL}$ (Low);

ABSOLUTE MAXIMUM RATINGS *Note1

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage (Digital)	IOV_{CC}-GND	-0.3	4.6	V
Supply Voltage (Analog)	V_{CI}-GND	-0.3	4.6	V
Driver Supply Voltage Range	DDV_{DH}-GND	-0.3	6.0	V
	V_{COMH}-V_{COML}	-0.3	6.0	V
	GND-V_{CL}	-0.3	4.6	V
	DDV_{DH}-V_{CL}	-0.3	9.0	V
	V_{GH}-V_{GL}	-0.3	30.0	V
Input Voltage	V_t	-0.3	IOV_{CC} +0.3	V
Operating Temperature	See page 8			
Storage Temperature				

PIN CONFIGURATION

PIN	SYMBOL	SIGNAL DESCRIPTION
1-4	DB_{17}-DB_0	Data Bus
5	GND	Ground
6	V_{CC}	Power Supply
7	/CS	Chip Select Signal
8	RS	Register Select Signal
9	/WR	Write Strobe Signal and Enables an Operation to Write Data when the Signal is low.
10	/RD	
11	IMO	Select the MPU System Interface Mode.
12-15	XL,YU,XR,YD (NC)	No Connection
16	LED_A	LED Backlight
17	LED_K_1	LED Backlight
18	LED_K_2	LED Backlight
19	LED_K_3	LED Backlight
20	LED_K_4	LED Backlight
21	IM_3	Select the MPU System Interface Mode
22	DB_4	Data Bus
23-30	DB_8-DB_{15}	Data Bus
31	RESET	Reset Pin
32-33	V_{CC}	Power Supply
34	GND	Ground
35	DB_5	Data Bus
36	DB_6	Data Bus
37	DB_7	Data Bus

ELECTRICAL CHARACTERISTICS, Ta = 25°C

ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
TFT Gate ON Voltage	V_{GH}			15.0		V
TFT Gate OFF Voltage	V_{GL}	Ta=+25°C		-8.0		V
TFT Common Electrode Voltage	V_{comH} V_{comL}		2.5 -2.0		4.5 0	V

Note (2): V_{com} must be adjusted to optimize display quality: cross talk, contrast ratio and etc.
Note (3): V_{GH} is TFT gate operating voltage.
Note (4): V_{GL} is TFT gate operating voltage. The storage capacitance structure of this products is C_{st} (Storage on Common). The low voltage level of V_{GL} signal must be fluctuated with same phase as V_{com}, in case of Storage on Gate structure.
Note (5): Environmental condition: 25°C±5°C.
Note (6): Operating Voltage V_{CC}=2.8V

BACKLIGHTING CHARACTERISTICS, Ta = 25°C, LED

ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
Forward Voltage	V_f	I_F=60mA	2.9	3.2	3.4	V
Reverse Current	I_r	V_f=5.0V			50	µA
Luminance	L_V	I_F=60mA	3500	3800		cd/m^2
Average	Avg		80			%
Colour Coordinate	X		0.24		0.30	
	Y		0.24		0.30	

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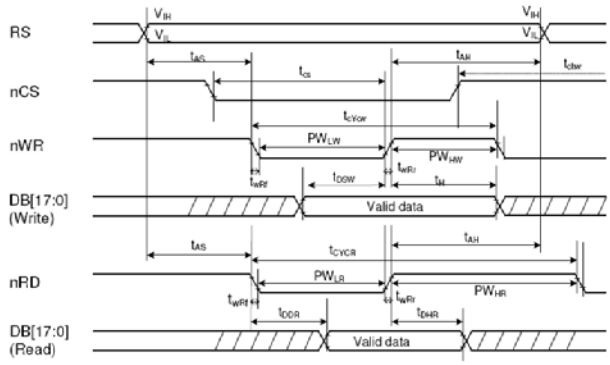
INTERFACE TIMING CHARACTERISTICS

Normal Write Mode IOV_{CC}=1.65V to 3.3V

I80-System Interface Timing Chracteristics



PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Bus Cycle Time	Write	t_{CYCW}		80		ns
	Read	t_{CYCR}		300		ns
Write Low Level Pulse Width		PW_{LW}		50		ns
Write High Level Pulse Width		PW_{HW}		15		ns
Read Low Level Pulse Width		PW_{LR}		150		ns
Read High Level Pulse Width		PW_{HR}		150		ns
Write / Read Rise/Fall Time		t_{WRr}/t_{WRf}			25	ns
Setup Time	Write	t_{AS}	RS to nCS, E/nWR	10		ns
	Read		RS to nCS, RW/nRD	5		ns
Address Hold Time		t_{AH}		5		ns
Write Data Setup Time		t_{DSW}		10		ns
Write Data Hold Time		t_H		15		ns
Read Data Delay Time		t_{DDR}			100	ns
Read Data Hold Time		t_{DHR}		20	100	ns